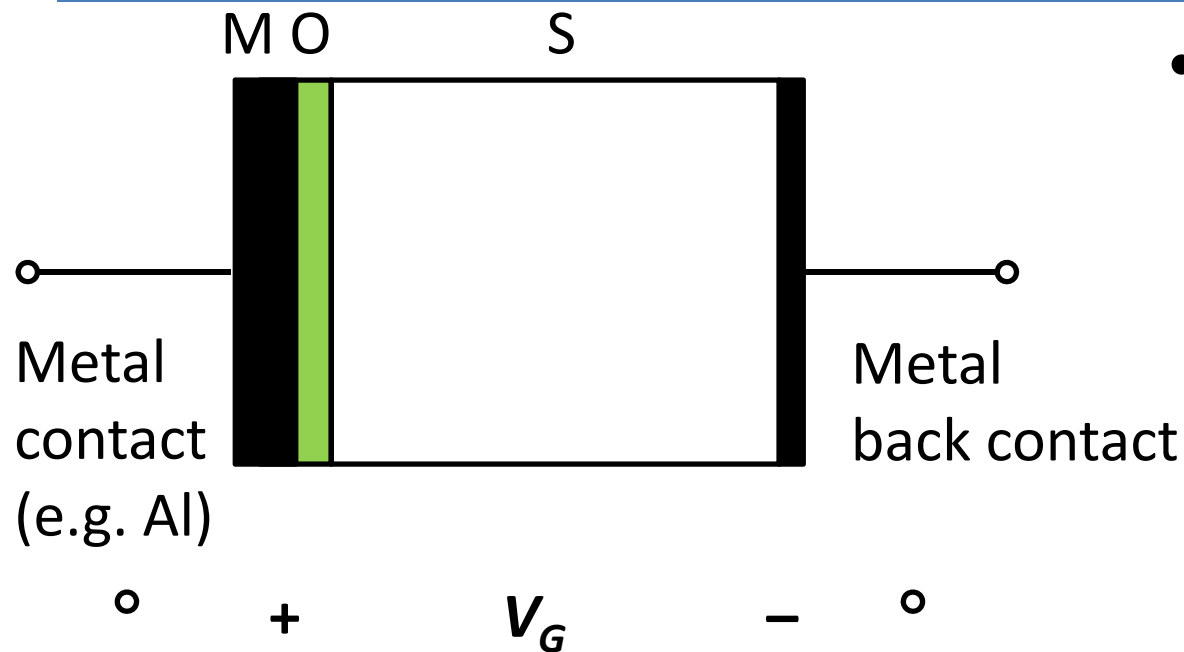


# Announcements

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- HW 4 posted, due Friday (May 2)
- Exams returned later this week.

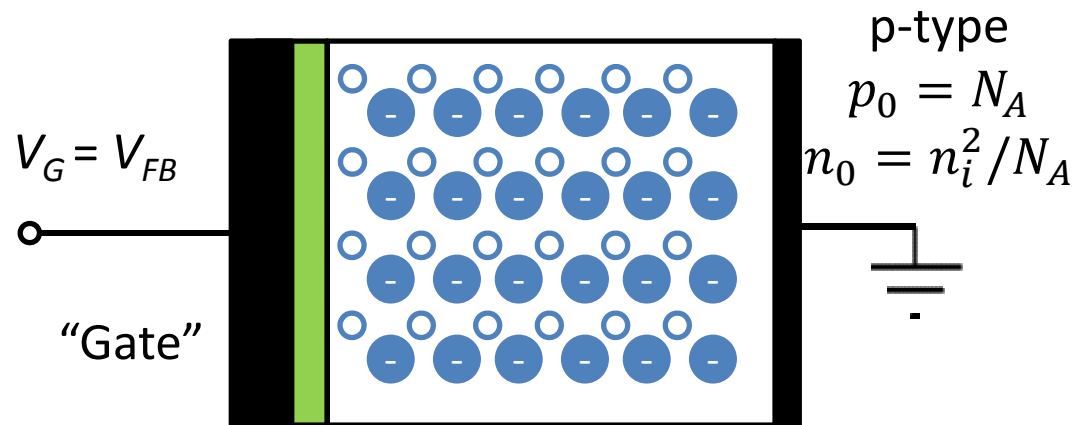
# MOS Capacitor



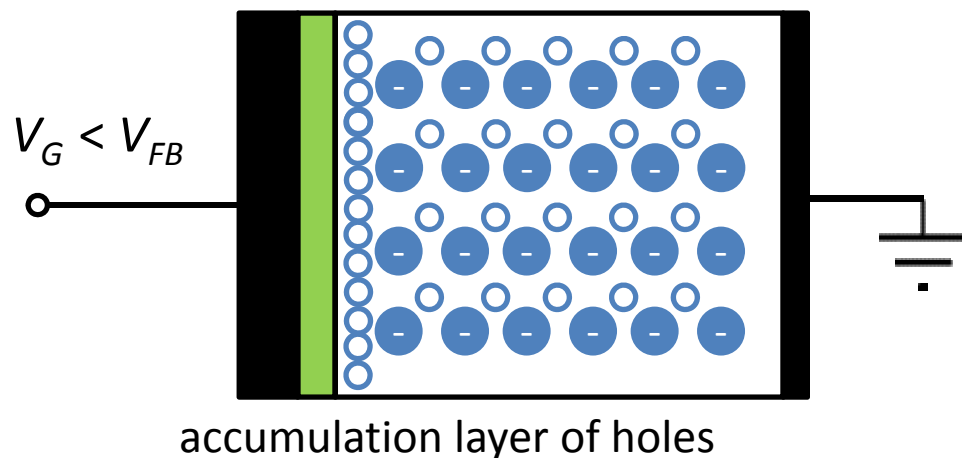
- Built-in voltage just like pn junction --- electrons shift to material with lower energy until balance reached.

- When external voltage is applied, electrons are attracted to higher voltage (+) and holes are attracted to lower voltage (-)
- Oxide layer blocks electrons or holes (isolation)

# MOS Capacitor Physics (p-Si)

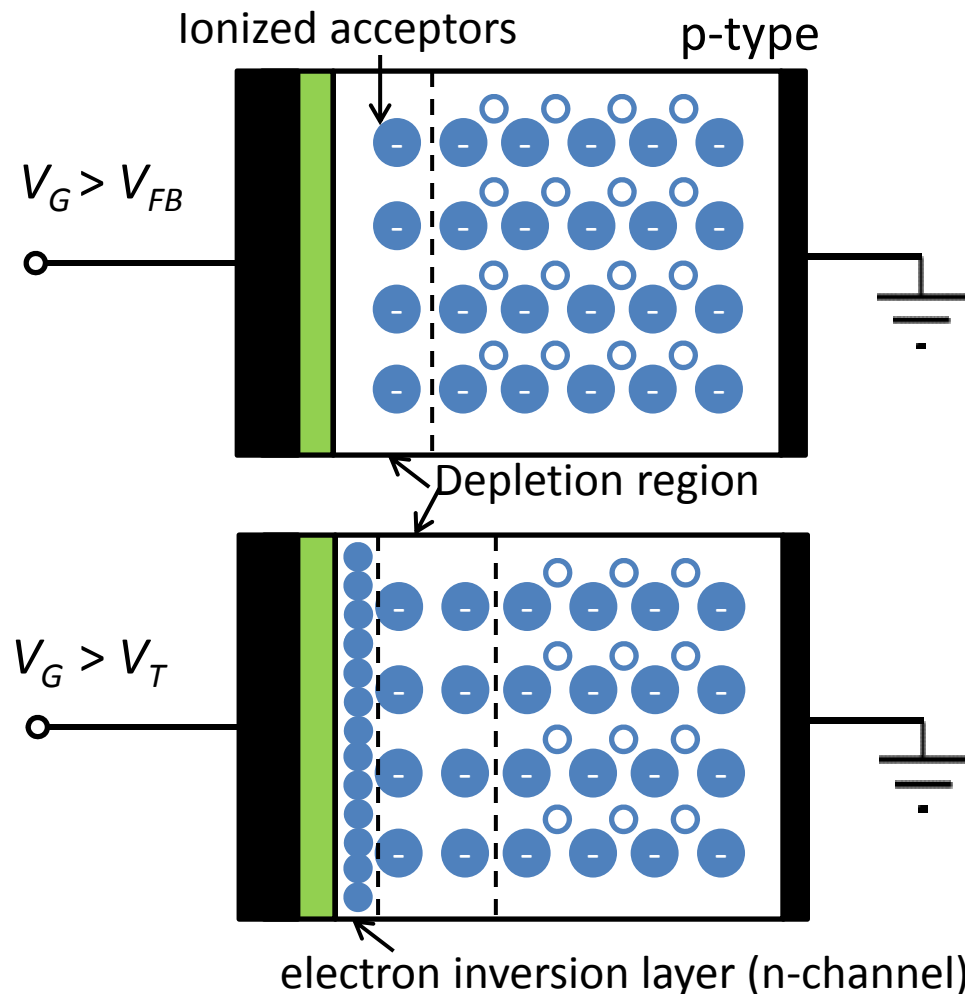


Flat Band ( $V_{FB} = \Phi_{BI}$ )  
When  $V_G = V_{FB}$ , hole concentration in Si equals doping (no net charge)



$V_G < V_{FB}$ , holes attracted to the gate side, but blocked by the oxide layer => **accumulation** of holes in semiconductor near interface with oxide.

# MOS Capacitor Physics (p-Si)

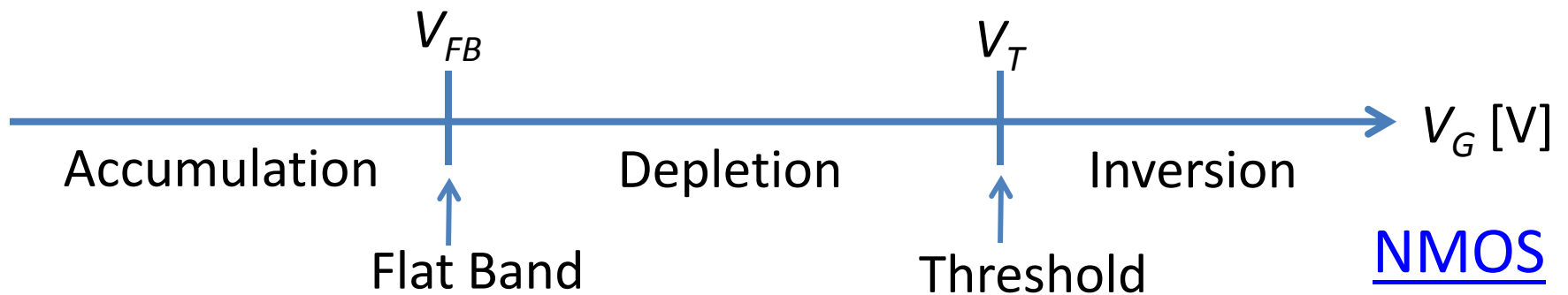


$V_G > V_{FB}$ , holes repelled from the O-S interface =>  
**Depletion** of holes in semiconductor near the interface with oxide.

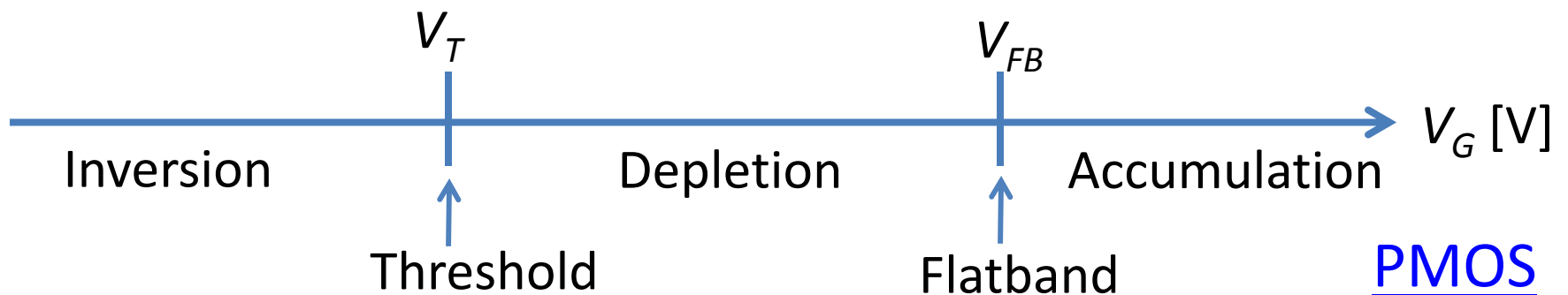
Further increasing  $V_G$  to  $V_G > V_T$ , electrons generated and attracted to the interface become the majority carrier => electron **inversion** layer formed in semiconductor just beneath the interface w/ oxide

# MOS Capacitor Physics

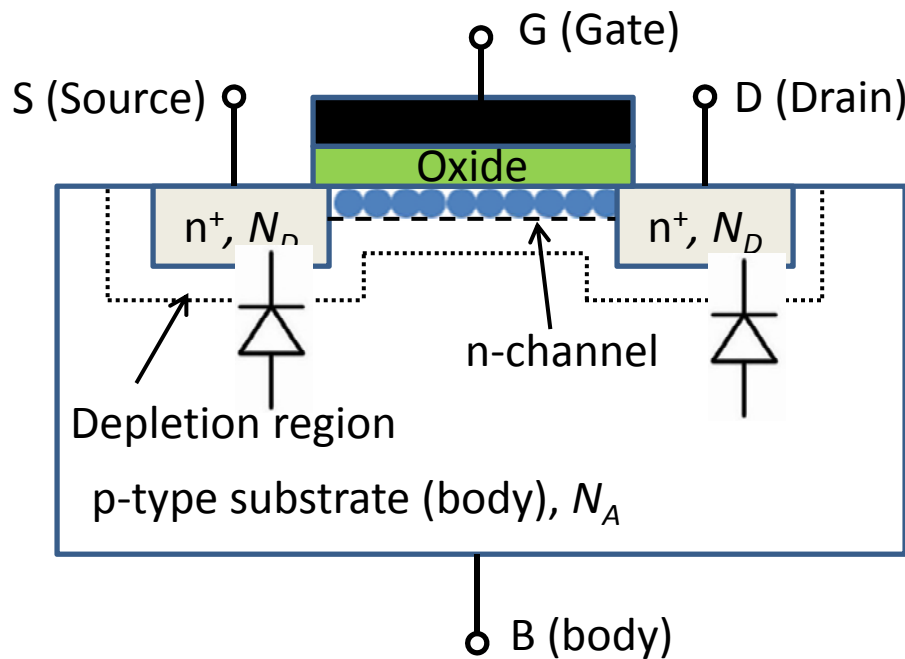
p-type semiconductor substrate (as in n-channel MOSFET)



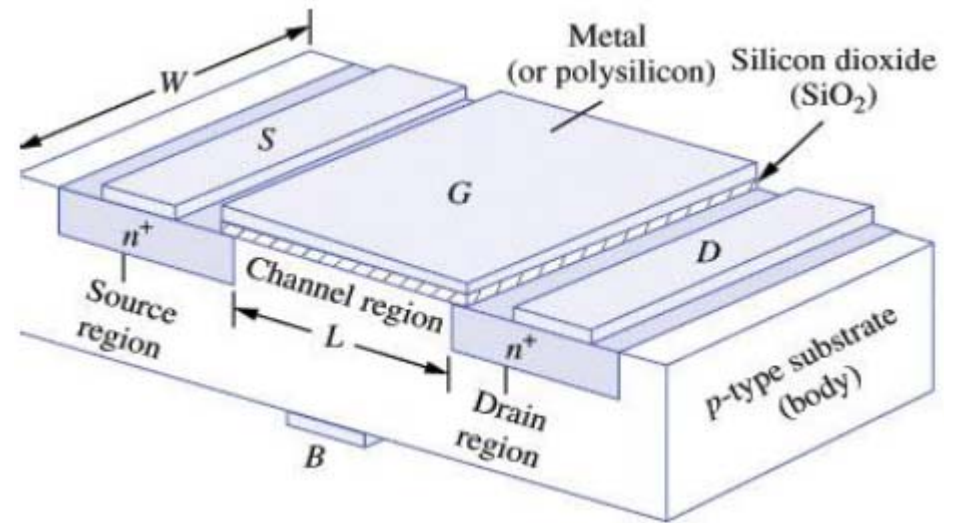
n-type semiconductor substrate (as in p-channel MOSFET)



# n-MOSFET

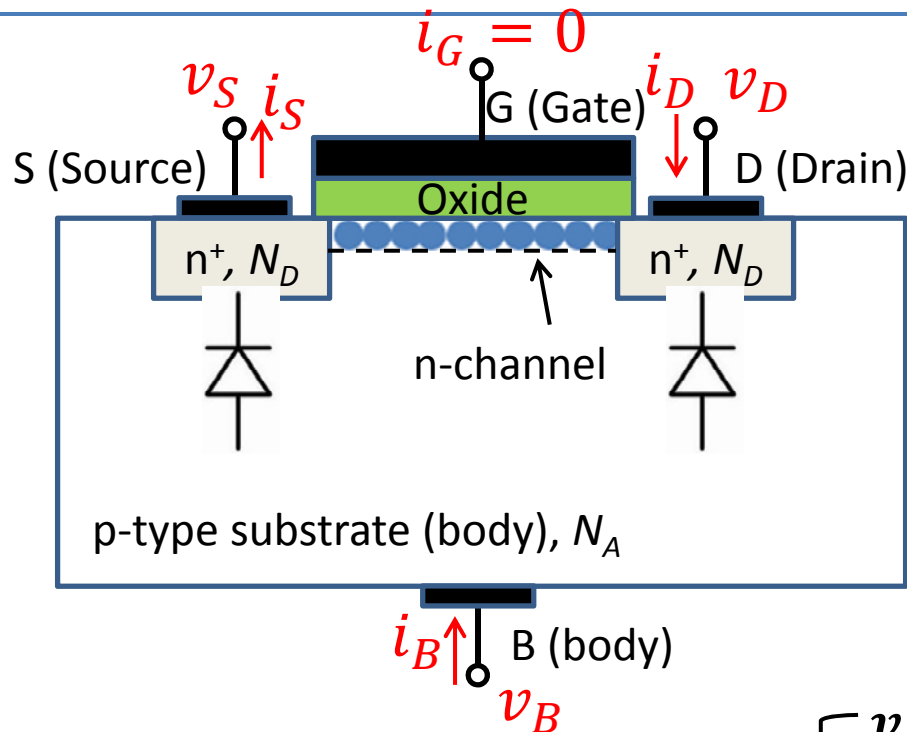


When  $V_G > V_T$ , an n-channel is formed between source (D) and drain (S).

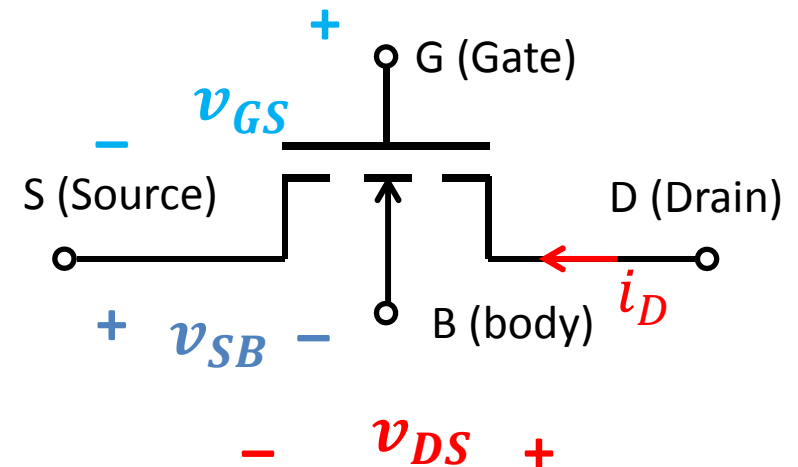


4 device terminals:  
Gate(G), Drain(D), Source(S) and Body(B).  
Source and drain regions form  $p$ - $n$  junctions with substrate ( $V_{SB} \geq 0$ )

# n-MOSFET



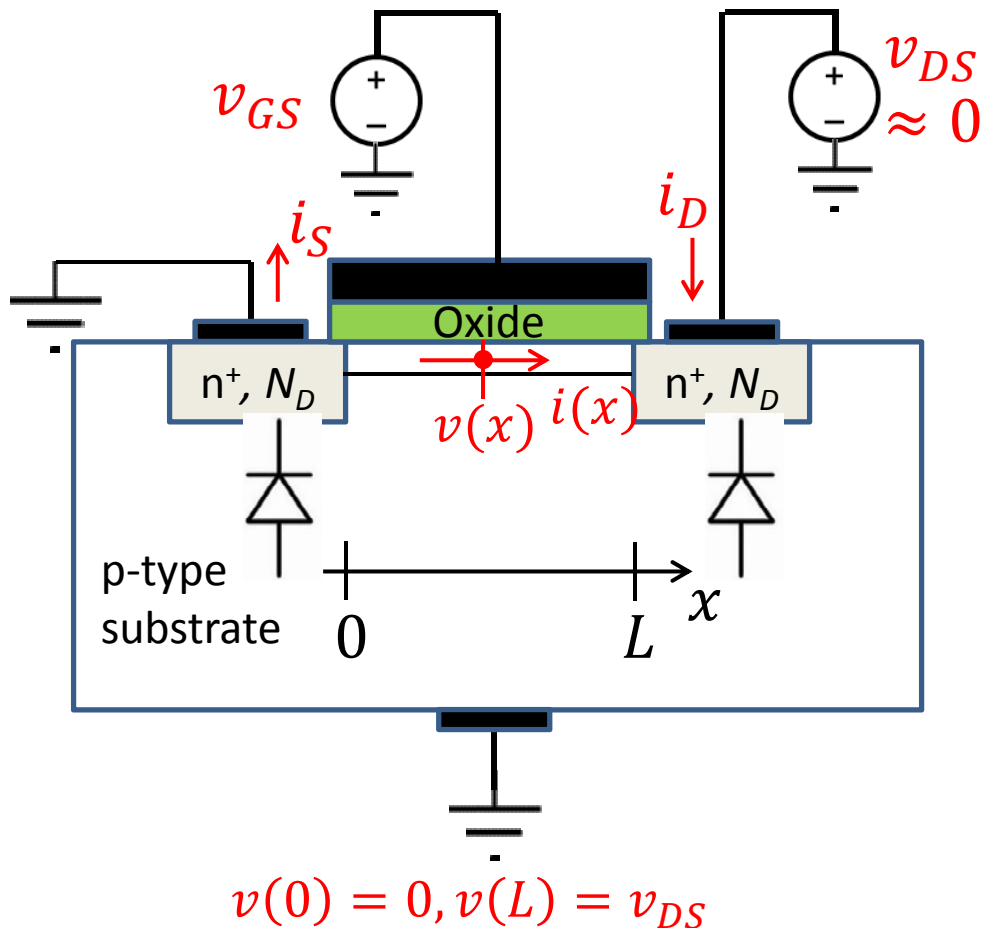
$$i_G, i_B \approx 0 \Rightarrow i_D = i_S$$



Device state:  $(v_{GS}, v_{DS}, v_{SB})$  {   
 $v_{GS}$ : Transfer characteristics   
 $v_{DS}$ : Output characteristics   
 $v_{SB}$ : body-effect (higher order effect)

Want to describe:  $i_D = f(v_{GS}, v_{DS}, v_{SB})$

# n-MOSFET Analysis (Triode)



- Goal: Find  $i_D = f(v_{GS}, v_{DS})$  when  $v_{DS}$  is small and  $v_{SB} = 0$
- Inversion charge per area at any point in the channel:

$$Q'' = -C_{ox}''(v_{GC} - V_{TN}) = -C_{ox}''(v_{GS} - v(x) - V_{TN}) \quad (1)$$

- Current in the channel:

$$i(x) = WQ''(x)(-\mu_n E_x) \quad (2)$$

- Electric field:

$$E_x = -\frac{dv(x)}{dx} \quad (3)$$

# n-MOSFET Analysis (Triode)

- Combining ①②③:

$$i(x) = -\mu_n C_{ox}'' W (v_{GS} - v(x) - V_{TN}) \frac{dv(x)}{dx}$$

- Integrate between 0 and  $L$ :  $v(0) = 0, v(L) = v_{DS}$

$$\int_0^L i(x) dx = \int_0^{v_{DS}} -\mu_n C_{ox}'' W (v_{GS} - v(x) - V_{TN}) dv(x)$$

- Current must be equal in the channel:  $i(x) = -i_D$  [Notice the sign!]

- We get the triode region formula:

$$i_D = K_n' \frac{W}{L} \left( v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS} \text{ where } K_n' = \mu_n C_{ox}''.$$

- The channel exists as long as  $v_{GC} = v_{GS} - v(x) > V_{TN}$  for all  $0 < x < L$ . This requires  $v_{GS} \geq v(x)_{\max} + V_{TN} = v_{DS} + V_{TN}$
- Thus the condition for triode region operation is:  $v_{GS} - v_{DS} \geq V_{TN}$

# Important Parameters

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- $K'_n$ : Process transconductance parameter
  - $K'_n = \mu_n C''_{ox}$  [A/V<sup>2</sup>] (fixed for a given technology)
- $K_n$ : Device transconductance parameter
  - $K_n = K'_n \frac{W}{L}$  [A/V<sup>2</sup>] (related to device dimensions)
- $\mu_n$ : electron mobility in the channel [cm<sup>2</sup>/V-s], generally lower than in bulk (surface scattering).
- $C''_{ox}$ : oxide capacitance per unit area [F/cm<sup>2</sup>]
  - $C''_{ox} = \epsilon_{ox}/T_{ox}$
  - $\epsilon_{ox}$ : oxide permittivity [F/cm]
  - $\epsilon_{ox} = \epsilon_r \epsilon_0 = 3.9\epsilon_0$  ( $\epsilon_r = 11.7$  for Si, 3.9 for SiO<sub>2</sub>)
  - $T_{ox}$ : oxide thickness [cm]

# Triode Region I-V Characteristics

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$$i_D = K'_n \frac{W}{L} \left( v_{GS} - V_{TN} - \frac{v_{DS}}{2} \right) v_{DS}$$

- When  $v_{DS}$  is small, ignore 2<sup>nd</sup> order terms

$$i_D = K'_n \frac{W}{L} (v_{GS} - V_{TN}) v_{DS}$$

- $i_D$  proportional to  $v_{DS} \Rightarrow$  the MOSFET is like a resistor (resistor value controlled by  $v_{GS}$ )
- On-resistance:

$$R_{on} = \left( \frac{\partial i_D}{\partial v_{DS}} \right)^{-1} = \frac{1}{K'_n \frac{W}{L} (v_{GS} - V_{TN})}$$